REMARKS

Reconsideration of the above-identified application in view of the preceding amendments and following remarks is respectfully requested. Claims 1-9 are pending in this application. Claim 1 has been amended to address a punctuation omission, namely including a comma at the end of the first limitation.

Applicant's representative would like to thank Examiner Pham for the courtesies extended during our recent telephone conversations. During our conferences, the applicant's representative conferred with Examiner Pham to discuss the novel and patentable structure of the subject application. Namely, an electrode portion (i.e., the N+ type diffusion layer) of a N+ type buried layer being located in an active region of a power transistor surrounded from all around by a plurality of vertical PNP transistors and the N+ type diffusion layer contacts the N+ type buried layer. This N+ type buried layer is formed to isolate a P type silicon substrate and the plurality of vertical PNP transistors. More particularly, we discussed the novelty of the electrode portion in section "a" (in Fig. 1 of the subject application) of the N+ type buried layer being located in the active region of a power transistor surrounded from all around by the plurality of vertical PNP transistors.

In the Office Action, Claims 1-8 were rejected under 35 U.S.C. § 103 (a) over the AAPA in view of U.S. Patent No. 5,121,185 to Tamba et al. The Examiner's grounds for rejection are herewith traversed, and reconsideration is respectfully requested.

The AAPA merely discloses a N^+ type electrode layer 118 outside the active region of a power transistor.

The Office Action combines the AAPA with Tamba et al. This is not proper because it is impossible and one of ordinary skill in the art would not make such a

combination. For example, the collector electrode 42 of the vertical PNP transistor of Tamba et al. is equivalent to a collector electrode such as the P+ type collector buried layer 3 and the P+ type collector layer 6 shown in Fig. 2 of the subject application. Thus, it is impossible to combine the collector electrode 42 of Tamba et al. with the AAPA. In the AAPA, a collector electrode is the P+ type collector buried layer 103 and a P+ type collector layer 106 in Fig. 4. Accordingly, one would not and cannot add the collector electrode 42 of tamba et al. because the AAPA (Fig. 4) already has the collector electrode in the form of the P+ type collector buried layer 103 and the P+ type collector layer 106. Thus, the combination is improper. Thus, the rejection is improper and allowance of the subject claims is respectfully requested.

For the sake of argument, the combination is further addressed. The N+ type diffusion layer of the subject application contacts the N+ type buried layer formed to isolate the P-type silicon substrate and the plurality of vertical PNP transistors. In contrast, the collector electrode 42 of Tamba et al. never contacts any buried layer. Moreover, an electrode portion (i.e., the N+ type diffusion layer) of an N+ type buried layer 2 of the subject application is not a collector electrode, while the collector electrode 42 of Tamba et al. is a collector electrode itself. For these reasons, the claimed structure is not present in the prior art combination.

The Office Action states that the N+ type embedded region 42 of the Tamba et al.'s vertical transistor corresponds to a N+ type diffusion layer (such as item 15 in Fig. 2 of the subject application). This is not correct. Rather, the vertical portion of N+ type embedded region 42 in Tamba et al. corresponds to a P+ type collector layer 6 in Fig. 2 of the subject application although the conductive types are reversed. Further, both the

horizontal portion of N+ type embedded region 42 and collector region 87 of Tamba et al. correspond to a P+ type collector buried layer 3 in Fig. 2 of the subject application (again conductive types are reversed). A N+ type emitter region 85 of Tamba et al. corresponds to a P+ type emitter layer 7 of Fig. 2 of the subject application and a P+ type base region of Tamba et al. corresponds to a N+ type base layer 8 in Fig. 2 of the subject application (again conductive types are reversed). Consequently, Tamba et al. merely disclose a vertical NPN transistor. Tamba et al. do not teach an N+ type buried layer 2 separating a P type silicon substrate 1 (herein, reference numerals included to the subject application are just for convenience and in no way to be considered limiting of the subject claims). Nor does Tamba et al. suggest an electrode portion like 15 and 18 of the N+ type buried layer 2 in the subject application and as recited in the pending claims.

Even further, Tamba et al. do not suggest the N+ type diffusion layer 15 being part of the electrode portion 18 and 15 as in Claim 1. It is clear that a collector electrode of the vertical NPN transistor of Tamba et al. was confused with the electrode portion 18 and 15 of the N+ type buried layer 2 of the structure of Claim 1. The collector electrode 42 of Tamba et al. never contacts any buried layer.

Lastly, Tamba et al. does not teach having the electrode portion 18 and 15 of the N+ type buried layer 2 surrounded from all around by the plurality of vertical PNP transistors located on the N+ type buried layer 2 and the AAPA does not cure any of these deficiencies.

In view of the above, there is nothing in either of these references that discloses or suggests, either alone or in combination, in whole or in part, the device defined by Claim 1 of the subject application. In particular for Claim 1, neither the AAPA nor Tamba et al.

disclose or suggest, either alone or in combination, in whole or in part, a power transistor including a plurality of vertical PNP transistors formed on a P-type silicon substrate, an N^+ type buried layer formed to isolate the P-type silicon substrate and the plurality of vertical PNP transistors from each other, and at least one electrode portion of the N^+ type buried layer, which has an N^+ type diffusion layer contacting the N^+ type buried layer, wherein the at least one electrode portion is located in an active region of the power transistor surrounded from all around by the vertical PNP transistors. Consequently, Claim 1 has a structure that is not shown or suggested in the prior art. Thus, Claim 1 and each of the claims depending therefrom are not rendered obvious by the combination of references cited by the Examiner and withdrawal of the rejection under 35 U.S.C. §103 (a) is respectfully requested.

In the Office Action, Claim 9 was rejected under 35 U.S.C. § 103 (a) over the AAPA in view of U.S. Patent No. 5,648,281 to Williams et al. The Examiner's grounds for rejection are herewith traversed, and reconsideration is respectfully requested.

The AAPA merely discloses a N^+ type electrode layer 118 outside the active region of a power transistor.

In the Office Action, a N+ sinker 348 of Williams et al. is equated to the N+ type diffusion layer 15, which is between a P+ type isolation layer 16 and a P+ type collector layer 6 and surrounding the the vertical PNP transistors from all around as shown in Fig. 2 of the subject application. However, the N+ sinker 348 is simply not an N+ type diffusion layer 15 at all. The N+ type diffusion layer as claimed is disposed between the vertical PNP transistors and contacts the N+ type buried layer 2 as shown in the central region of Fig. 2 of the subject application. The N+ diffusion layer 15 of claim 15 does not

surround the vertical PNP transistors from all around but rather is surrounded from all around by the P+ type collector layers 6 of the vertical PNP transistors. Williams et al. do not suggest, let alone teach, such a structure.

Further, neither the AAPA nor Williams et al. disclose the N+ type diffusion layer 15 of the electrode portion 15, 18 passing between P type collector buried layers 3 as recited in Claim 9.

Lastly, none of the prior art references have an N+ type diffusion layer being an electrode portion of a N+ type buried layer and contacting the N+ type buried layer located in an active region of a plurality of vertical PNP transistors as is necessary when surrounded from all around by the plurality of vertical PNP transistors.

In view of the above, there is nothing in either of these references that discloses or suggests, either alone or in combination, in whole or in part, the device defined by Claim 9 of the subject application.

In particular for Claim 9, neither the AAPA nor Williams et al. disclose or suggest, either alone or in combination, in whole or in part, a power transistor having suppression of problematic leak current, the power transistor including a plurality of vertical PNP transistors formed on a P-type substrate, each PNP transistor having a P^+ type collector, an N+ type base well formed at a base region, a P^+ type emitter layer and an N^+ type base layer, P^+ type collector buried layers formed under the N^+ type base well, an N^+ type buried layer isolating the P-type substrate from the P^+ type collector, an N-type epitaxial layer formed over a surface of the P-type substrate, an N^+ type electrode layer, and a plurality of N^+ type diffusion layers formed at electrode portions within an active region under, contacting and surrounding the N^+ type electrode layer to reduce resistance of the

N-type epitaxial layer by extending therethrough to contact the N^+ type buried layer, wherein at least one of the N^+ type diffusion layers passes between the P^+ type collector buried layers. Neither of the cited references disclose such an arrangement of features. Thus, there is nothing in either of these references that discloses or suggests, either alone or in combination, in whole or in part, the device defined by Claim 9 of the subject application. Thus, for at least these reasons, Claim 9 is not obvious in view of the cited combination and allowance is respectfully requested.

It is respectfully submitted that all of the claims in this application, namely Claims 1-9, are in condition for allowance, and such action is earnestly solicited. Any additional fees or overpayments due as a result of filing the present paper may be applied to Deposit Account No. 04-1105.

If after reviewing this amendment, the Examiner believes that a telephone interview would facilitate the resolution of any remaining matters the undersigned attorney may be contacted at the number set forth herein below.

Respectfully submitted,

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